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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,324	12/04/2003	Debendra Mallik	P16831	7342

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EXAMINER	
ANDUJAR, LEONARDO	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,324	MALLIK ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *11-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/04/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of group I in the reply filed on 05/05/2005 is acknowledged. The traversal is on the ground(s) that process including the step suggested in the election restriction sent on 042/1/2005 would not be materially different from the group II process claim. This is not found persuasive because referring to the restriction requirement set forth in the Office Action sent on 04/21/2005, it clearly shows that the alternative method proposed by the examiner would be distinct from the process claimed in claim 11. Note that the process of claim 11 does not recite any double data rate memory, which is a structural limitation, recited in claim 15. Furthermore, the inventions are distinct if either (emphasis added) or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). The requirement is still deemed proper and is therefore made FINAL.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the underfill material disposed between the first face of each of the plurality of integrated circuit die and the integrated circuit package substrate must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurita (US 2002/0135057).

5. Regarding claim 1, Kurita (e.g. figs. 2e and 3) shows an apparatus comprising: an integrated circuit die; an integrated circuit package 3 coupled to the integrated circuit die 1; mold compound 7 in contact with the integrated circuit die and the integrated circuit package; and an interconnect 6 coupled to the integrated circuit package, wherein a first portion (middle portion) of the interconnect is in contact with the mold compound, wherein a second portion (top surface) of the interconnect is not in contact with the mold compound, and wherein a third portion (bottom surface) of the interconnect is in contact with the integrated circuit package.

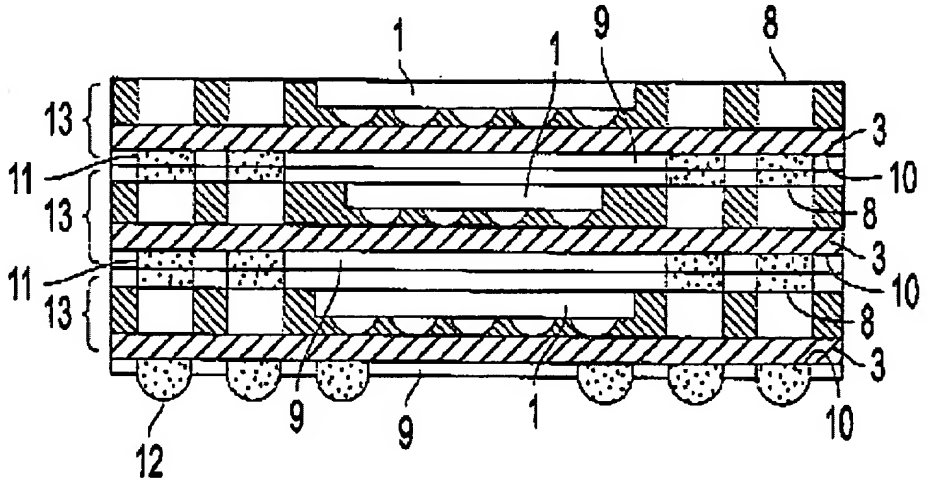

FIG. 3

6. Regarding claim 2, Kurita shows the second portion is an upper portion of the interconnect and the third portion is a lower portion of the interconnect.

7. Regarding claim 3, Kurita shows a second integrated circuit package 3 (second substrate in upward direction); a second interconnect 6 coupled to the second integrated circuit package, wherein the second interconnect is coupled to the first interconnect.

8. Regarding claim 4, Kurita shows a the second integrated circuit package is coupled to the mold compound (e.g. thermally).

9. Regarding claim 5, Kurita shows a second integrated circuit die 1 coupled to the second integrated circuit package; second mold compound 7 in contact with the second integrated circuit die and the second integrated circuit package; and a third interconnect 6 coupled to the second integrated circuit package, wherein a first portion (middle portion) of the third interconnect is in contact with the second mold compound, and wherein a second portion (top surface) of the third interconnect is not in contact with the second mold compound, and wherein a third portion (bottom surface) of the third interconnect is in contact with the second integrated circuit package.

10. Regarding claim 6, Kurita shows a third integrated circuit package 3 (third package in upward direction); a fourth interconnect 6 coupled to the third integrated circuit package, wherein the fourth interconnect is coupled to the third interconnect (electrically).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurita (US 2002/0135057) in view of Takiar (US 5,422,435).

13. Regarding clam 7, Kurita shows most aspects of the instant invention except for a second integrated circuit coupled to the integrated circuit die, in contact with the mold compound, and electrically couple the integrated circuit package. Takiar (e.g. fig. 1) shows a package comprising a stacked arrangement of semiconductor dies that provide a single circuit assembly. As shown in figure 1, a second integrated circuit die 24 is coupled to a first integrated circuit die 22 is in contact with the mold compound 25, and is electrically couple the integrated circuit package 40. According to Takiar, this type of arrangement is used to decrease the size and weight of the device, as well as to improve its performance (col. 2/lls. 3-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device disclosed by Kurita having two or more semiconductor dies wherein the second integrated circuit die is coupled to the first integrated circuit die, in contact with the mold compound, and electrically couple the integrated circuit package in order to provide a single circuit assembly having a decreased size and weight as suggested by Takiar.

14. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over McDavid (US 5,040,052) in view of Kurita (US 2002/0135057).

15. Regarding claim 8, McDavid (e.g. fig. 4) shows an apparatus comprising an integrated circuit package substrate 11 and a plurality of integrated circuit die 12 coupled to the integrated circuit package substrate. McDavid does not show that the apparatus includes a mold compound in contact with the plurality of integrated circuit die and the integrated circuit package substrate; and an interconnect coupled to the integrated circuit package substrate and electrically coupled to one of the plurality of

integrated circuit die, wherein a first portion of the interconnect is in contact with the mold compound, wherein a second portion of the interconnect is not in contact with the mold compound, and wherein a third portion of the interconnect is in contact with the integrated circuit package. Nevertheless, Kurita (e.g. figs. 2e and 3) shows an apparatus comprising: an integrated circuit die 1 coupled to an integrated circuit package substrate 1; a mold compound 7 in contact with the integrated circuit die and the integrated circuit package; and an interconnect 6 coupled to the integrated circuit package substrate and electrically coupled to the integrated circuit die, wherein a first portion (middle portion) of the interconnect is in contact with the mold compound, wherein a second portion (top surface) of the interconnect is not in contact with the mold compound, and wherein a third portion (bottom surface) of the interconnect is in contact with the integrated circuit package substrate. Also, Kurita teaches that this type of embodiment enable a thin construction and greater degree of freedom in design (0020). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the apparatus disclosed by McDavid a mold compound in contact with the integrated circuit dies and the integrated circuit package; and an interconnect coupled to the integrated circuit package substrate and electrically coupled to the integrated circuit dies, wherein a first portion of the interconnect is in contact with the mold compound, wherein a second portion of the interconnect is not in contact with the mold compound, and wherein a third portion of the interconnect is in contact with the integrated circuit package to provide a semiconductor package having a thin construction and greater degree of freedom in design as suggested by Kurita.

16. Regarding claim 9, McDavid in view of Kurita shows a underfill material disposed between the first face of each of the plurality of integrated circuit die and the integrated circuit package substrate.

17. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over McDavid (US 5,040,052) in view of Kurita (US 2002/0135057) further in view of Takiar (US 5,422,435).

18. Regarding clam 10, McDavid in view Kurita shows most aspects of the instant invention except for a second integrated circuit coupled to the integrated circuit die, in contact with the mold compound, and electrically couple the integrated circuit package. Takiar (e.g. fig. 1) shows a package comprising a stacked arrangement of semiconductor dies that provide a single circuit assembly. As shown in figure 1, a second integrated circuit die 24 is coupled to a first integrated circuit die 22 is in contact with the mold compound 25, and is electrically couple the integrated circuit package 40. According to Takiar, this type of arrangement is used to decrease the size and weight of the device, as well as to improve its performance (col. 2/lls. 3-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device disclosed by McDavid in view Kurita having two or more semiconductor dies wherein the second integrated circuit die is coupled to the first integrated circuit die, in contact with the mold compound, and electrically couple the integrated circuit package in order to provide a single circuit assembly having a decreased size and weight as suggested by Takiar.

19. Claims 15-17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurita (US 2002/0135057) in view of Chang (US 20020196650).

20. Regarding claim 15, Kurita shows a system (i.e. personal computer) including a an integrated circuit die 1; an integrated circuit package 3 coupled to the integrated circuit die; mold compound 7 in contact with the integrated circuit die and the integrated circuit package; and an interconnect 6 coupled to the integrated circuit package, wherein a first portion (middle portion) of the interconnect is in contact with the mold compound, wherein a second portion (top surface) of the interconnect is not in contact with the mold compound, and wherein a third portion (bottom surface) of the interconnect is in contact with the integrated circuit package (see figs. 2e and 3; pp 0005). Kurita does not show that the system includes a double data rate memory. Nevertheless, Chang teaches (e.g. fig. 2) a computer system including a double data rate memory (204-207) electrically coupled to an integrated circuit die 202. Chang teaches that under the mode of double data rate, the memory can perform data access control during both the raising edge and falling edge of the system clock signal. Thus, the operation speed of the memory is fastened (pps. 005, 006 & 0028). It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically couple a double data rate memory to the integrated circuit die disclosed by Kurita in order to increase the operation speed of the computer system as suggested by Chang.

21. Regarding claim 16, Kurita shows a second integrated circuit die 1 coupled to the second integrated circuit package; second mold compound 7 in contact with the second

integrated circuit die and the second integrated circuit package; and a second interconnect 6 coupled to the second integrated circuit package and the first interconnect.

22. Regarding claim 17, Kurita shows that the second circuit package in coupled to the mold compound (i.e. thermally).

23. Regarding claim 19, Chang shows a mother board 200 electrically coupled to the integrated circuit die and to the memory.

24. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurita (US 2002/0135057) in view of Chang (US 20020196650) further in view of Takiar (US 5,422,435).

25. Regarding clam 18, Kurita in view of Chang shows most aspects of the instant invention except for a second integrated circuit coupled to the integrated circuit die, in contact with the mold compound, and electrically couple the integrated circuit package. Takiar (e.g. fig. 1) shows a package comprising a stacked arrangement of semiconductor dies that provide a single circuit assembly. As shown in figure 1, a second integrated circuit die 24 is coupled to a first integrated circuit die 22 is in contact with the mold compound 25, and is electrically couple the integrated circuit package 40. According to Takiar, this type of arrangement is used to decrease the size and weight of the device, as well as to improve its performance (col. 2/lls. 3-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device disclosed by Kurita in view of Chang having two or more semiconductor dies wherein the second integrated circuit die is coupled to the first integrated circuit die, in

contact with the mold compound, and electrically couple the integrated circuit package in order to provide a single circuit assembly having a decreased size and weight as suggested by Takiar.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Taniguchi (US 6,489,676) teach similar structure to the instant invention.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Patent Examiner

Art Unit 2826
07/12/2005